REMARKS

Claims 1, 3, 4, 6-11, 13, 15, 17-21, 23, 24, 26, 28-31, 33, 34, 36, 38-40, 42, 43, 45, 47, and 48 are pending in the present application and stand rejected. Claims 1, 4, 6, 7, 10, 11, 15, 21, 24, 26, 31, 34, 36, 40, 43, and 45 are amended. No new matter has been added. The Examiner's reconsideration is respectfully requested in view of the above amendments and the following remarks.

Claim Rejections – 35 U.S.C. 103(a)

1. Claims 1, 3-4, 6-7, 9, 11, 15, 18-19, 21, 25-26, 29,31, 33-36, 39-40, 42-43, and 45 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Circello [US Pat # 5,872,940] in view of Ryan [US Pat Pub # 2006/0277424] and in further view of Funk [US Pat # 6,026,119], as set forth in pages 2-8 of the Final Office Action.

Claims 1 and 31

It is respectfully submitted that Circello, Ryan, and Funk, alone or in combination, do not disclose or suggest, *the first bus master controller includes a multiplexer configured to receive a command packet and a data packet and output one of the command packet or the data packet to the first common bus*, as essentially recited in amended claims 1 and 31.

For example, FIG. 4 of Applicant's disclosure illustrates multiplexer 420 and FIG. 11-12 of Applicant's disclosure illustrates an interleaving of command packets ["C"] and data packets ["D"] on databus DIO, which is connected to common bus 305.

Circello teaches a system bus controller 103 including multiplexers 510 and 502. However, as opposed to amended claims 1 and 31, multiplexers 510 and 502 do not receive a command packet and a data packet. For example, Circello teaches (in FIG. 5 and col. 4, lines 5-15) that multiplexer

510 only receives chip select register bits 604, 608, and 612 respectively from registers 603, 607, and 611. Further, Circello teaches (in FIG. 5 and col. 3, lines 60-col. 4, line 4) that multiplexer 502 only receives a R/W access signal and an inverted R/W access signal. Further, the output of each of the multiplexers 502 and 510 **do not** provide **one** of a command packet or a data packet to system bus 107. For example, Circello teaches (in FIG. 5 and col. 3, lines 21-22) that only a R/W access signal ERE is output from multiplexer 502.

The deficiencies of Circello with regard to a *first bus master controller includes a multiplexer configured to receive a command packet and a data packet and output one of the command packet or the data packet to the first common bus* are not cured by either Ryan or Funk. For example, Ryan and Funk do not disclose a multiplexer, much less a *multiplexer configured to receive a command packet and a data packet.*

For at least the foregoing reasons, Circello, Ryan, and Funk, alone or in combination, do not disclose or suggest claim 1 and 31. Thus, claims 1 and 31 are believed to be patentable over Circello, Ryan, and Funk.

Claim 11

It is further respectfully submitted that Circello, Ryan, and Funk, alone or in combination, do not disclose or suggest, *a first bus master controller connected to a plurality of external peripherals via a first common bus and a second bus master controller connected to the shared memory and a flash memory via a second common bus*, as essentially recited in amended claim 11.

The use of two common busses according to this embodiment facilitates access to flash memory while an external application (e.g., a camera) is controlled. This embodiment allows more

flexible memory control and more memory intensive operations, while the external application is controlled (See paragraph [0048] of Applicant's U.S. Patent Pub # 2005/0066074).

The Examiner concedes (in pages 3-4 of the Office Action) that Circello essentially fails to teach a shared memory connected to a second bus master controller. The Examiner suggests instead that either busmaster 246 or dma controller 250 of Ryan disclose a second bus master controller connected to a shared memory.

However, as opposed to amended claim 11, the busmaster 246 and the dma controller 250 of Ryan are not connected to a shared memory and a flash memory via a common bus.

For example, FIG. 3 of Ryan does **not** illustrate a connection between busmaster 246 and flash 222 using bus 240. Further, FIG. 3 of Ryan does **not** illustrate a connection between dma controller 250 and flash 222 using bus 240. Indeed, FIG. 3 of Ryan merely illustrates a direct connection between flash 222 and a static memory interface 210.

Moreover, FIG. 3 of Ryan does not illustrate a connection between busmaster 211 and flash 222 using bus 209. Further, FIG. 3 of Ryan does not illustrate a connection between controllers 212 or 214 and flash 222 using bus 209. The deficiencies of Circello and Ryan in this regard are not cured by Funk.

Further, even assuming *arguendo*, that Circello, Ryan, and Funk were combined, such a combination would not result in claim 11. For example, combining bus 209 or 240 from Ryan with bus 107 from Circello does not produce a second bus master controller connected to shared memory and a flash memory via second common bus because busses 209 and 240 are not connected to flash memories.

Claim 21

It is further respectfully submitted that Circello, Ryan, and Funk, alone or in combination, do not disclose or suggest, a *command packet includes a module device select signal used for selecting one of the plurality of external peripherals and an address specifying a start address of a data transfer*, as recited in amended claim 21. In this way, a single packet provides both peripheral selection information and address information. However, as shown in FIG. 1, Circello merely teaches **separate dedicated** lines for address and control signals.

The deficiencies of Circello with regard to a *command packet includes a module device select signal used for selecting one of the plurality of external peripherals and an address specifying a start address of a data transfer* are not cured by either Ryan or Funk. For example, Ryan merely teaches (in para. [0007]) a method of partitioning memory. Further, Funk merely discloses (in FIG. 1) a modem for transmitting packets.

Claim 40

Claim 40 is believed to be patentable over Circello, Ryan, and Funk for at least similar reasons to claims 1 and 31. For example, claim 40 has been amended to essentially recite *sending one of a data packet or a command packet commonly receivable by the plurality of external peripherals over the first common bus*. As discussed above, the output of each of the multiplexers 502 and 510 of Circello **do not** provide **one** of a command packet or a data packet to the system bus 107.

For at least the foregoing reasons, Circello, Ryan, and Funk, alone or in combination, do not disclose or suggest claim 1, 11, 21, and 31. Thus, claims 1, 11, 21, and 31 are believed to be patentable over Circello, Ryan, and Funk.

Moreover, claims 3-4, 6-7, 9, 15, 18-19, 21, 25-26, 29, 33-36, 39, 42-43 and 45 are believed to be patentable over Circello, Ryan, and Funk at least by virtue of their respective dependencies to their base independent claims.

2. Claims 8, 17, 28, 38, and 47 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Circello, Ryan, Funk, and in further view of Watanabe [US Pat # 6,378,102], as set forth in pages 8-9 of the Final Office Action.

3. Claims 10 and 20 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Circello, Ryan, Funk, and in further view of Fueki [US Pat Pub # 2002/0166058], as set forth in pages 9-11 of the Final Office Action.

4. Claim 13 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Circello, Ryan, Funk , and in further view of Wilska [US Pat Pub # 2002/0082043], as set forth in page 11 of the Final Office Action.

The above 103 rejections (i.e., 2-4) are premised, in part, on the Examiner's reliance on Circello, Ryan and Funk, as disclosing all elements of claim 1, 11, 21, 31, and 40, where claims 8 and 10 depend from claim 1, claims 13, 17, and 20 depend from claim 11, claim 28 depends from claim 21, claim 38 depends from claim 31, and claim 47 depends from claim 40.

However, Circello, Ryan and Funk do not disclose all of the limitations of claims 1, 11, 21, 31, and 40 for at least the reasons discussed above. Further, the deficiencies of Circello, Ryan and Funk in disclosing claims 1, 11, 21, 31, and 40 are not cured by Watanabe, Fueki, or Wilska. For example, at the very least, Watanabe, Fueki, and Wilska fail to disclose or suggest output of one of a command packet or a data packet to a common bus, a second bus master controller connected to the shared memory and a flash memory via second common bus, and a command packet including a

module device select signal used for selecting an external peripheral and an address specifying a start address of a data transfer.

Accordingly, the above respective combinations of Circello, Ryan, Funk, Watanabe, Fueki, and Wilska cannot render obvious any of the above claims rejected under 35 U.S.C. 103(a).

Conclusion

In view of the foregoing remarks, it is respectfully submitted that all the claims now pending in the application are in condition for allowance. Early and favorable reconsideration is respectfully requested.

Respectfully submitted,
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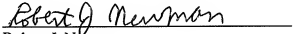

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